SCHOTTKY BIPOLAR LSI MICROCOMPUTER SET

3214 INTERRUPT CONTROL UNIT

The INTEL Bipolar Microcomputer Set is a family of Schottky bipolar LSI circuits which simplify the construction of microprogrammed central processors and device controllers. These processors and controllers are truly microprogrammed in the sense that their control logic is organized around a separate read-only memory called the microprogram memory. Control signals for the various processing elements are generated by the microinstructions contained in the microprogram memory. In the implementation of a typical central processor, as shown below, the microprogram interprets a higher level of instructions called macroinstructions, similar to those found in a small computer. For device controllers, the microprograms directly implement the required control functions.

The Intel 3214 Interrupt Control Unit (ICU) implements multi-level interrupt capability for systems designed with Series 3000 computing elements.

The ICU accepts an asynchronous interrupt strobe from the 3001 Microprogram Control Unit or a bit in microprogram memory and generates a synchronous interrupt acknowledge and an interrupt vector which may be directed to the MCU or CP Array to uniquely identify the interrupt source.

The ICU is fully expandable in 8-level increments and provides the following system capabilities:

- Eight unique priority levels per ICU
- Automatic Priority Determination
- Programmable Status
- N-level expansion capability
- Automatic interrupt vector generation

High Performance – 80 ns Cycle Time

Compatible with Intel 3001 MCU and 3002 CPE

8-Bit Priority Interrupt Request Latch

4-Bit Priority Status Latch

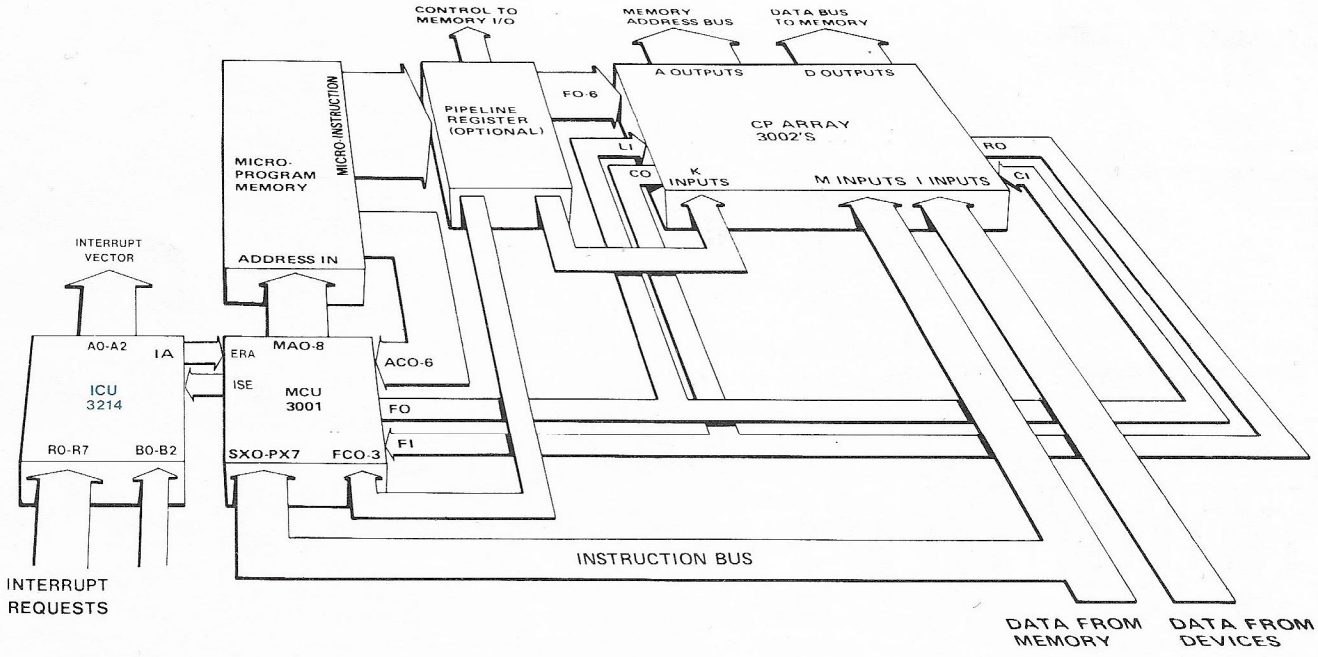
3-Bit Priority Encoder with Open Collector Outputs

DTL and TTL Compatible

8-Level Priority Comparator

Fully Expandable

24-Pin DIP



Other members of the INTEL Bipolar Microcomputer Set:

3001 Microprogram Control Unit	3212 Multi-Mode Latch Buffer	3304A Schottky Bipolar ROM (512 x 8)
3002 Central Processing Element	3226 Inverting Bi-Directional Bus Driver	3601 Schottky Bipolar PROM (256 x 4)
3003 Look-Ahead Carry Generator	3301A Schottky Bipolar ROM (256 x 4)	3604 Schottky Bipolar PROM (512 x 8)

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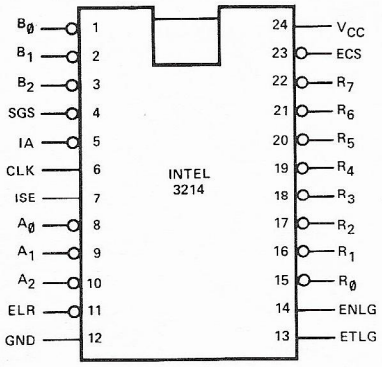
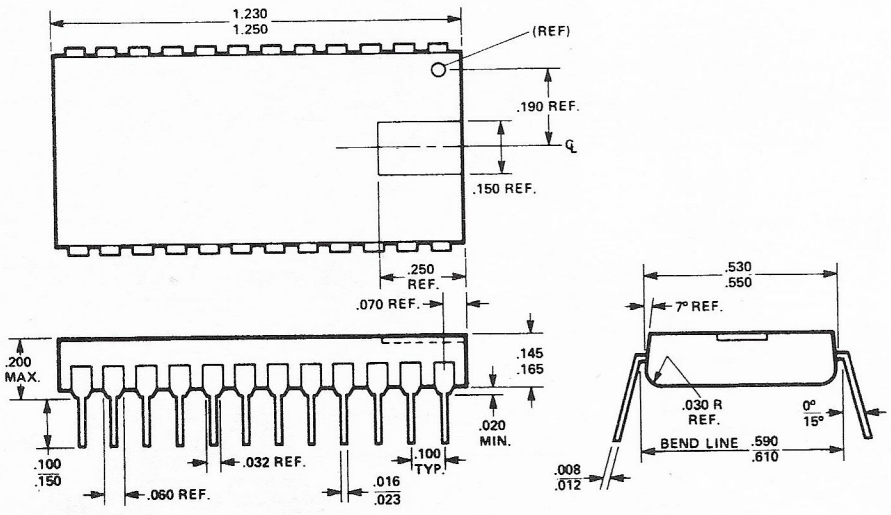
APPENDIX

PACKAGE CONFIGURATION



PACKAGE OUTLINE



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1–3	B_0–B_2	Current Status Inputs The Current Status inputs carry the binary value modulo 8 of the current priority level to the current status latch.	Active LOW
4	SGS	Status Group Select Input The Status Group Select input informs the ICU that the current priority level does belong to the group level assigned to the ICU.	Active LOW
5	IA	Interrupt Acknowledge The Interrupt Acknowledge Output will only be active from the ICU (multi-ICU system) which has received a priority request at a level superior to the current status. It signals the controlled device (usually the processor) and the other ICUs OR-tied on the Interrupt Acknowledge line that an interrupt request has been recognized. The IA signal also sets the Interrupt Disable flip-flop (it overrides the clear function of the ECS input).	Active LOW Open-Collector Output
6	CLK	Clock Input The Clock input is used to synchronize the interrupt acknowledge with the operation of the device which it controls.	
7	ISE	Interrupt Strobe Enable Input The Interrupt Strobe Enable input informs the ICU that it is authorized to enter the interrupt mode.	
8–10	A_0–A_2	Request Level Outputs When valid, the Request Level outputs carry the binary value (modulo 8) of the highest priority request present at the priority request inputs or stored in the priority request latch. The request level outputs can become active only with the ICU which has received the highest priority request with a level superior to the current status.	Active LOW Open-Collector
11	ELR	Enable Level Read Input When active, the Enable Level Read input enables the Request Level output buffers (A_0–A_2).	Active LOW
12	GND	Ground	
13	ETLG	Enable This Level Group Input The Enable This Level Group input allows a higher priority ICU in multi-ICU systems to inhibit interrupts within the next lower priority ICU (and all the following ICUs).	
14	ENLG	Enable Next Level Group Output The Enable Next Level Group output allows the ICU to inhibit interrupts within the lower priority ICU in a multi-ICU system.	
15–22	R_0–R_7	Priority Interrupt Request Inputs The Priority Interrupt Request inputs are the inputs of the priority Interrupt Request Latch. The lowest priority level interrupt request signal is attached to R_0 and the highest is attached to R_7.	Active LOW
23	ECS	Enable Current Status Input The Enable Current Status input controls the current status latch and the clear function of the Interrupt Inhibit flip-flop.	Active LOW
24	V_{CC}	+5 Volt Supply	

NOTE:
(1) Active HIGH, unless otherwise noted.

FUNCTIONAL AND LOGICAL DESCRIPTION

The ICU adds interrupt capability to suitably microprogrammed processors or controllers. One or more of these units allows external signals called interrupt requests to cause the processor/controller to suspend execution of the active process, save its status, and initiate execution of a new task as requested by the interrupt signal.

It is customary to strobe the ICU at the end of each instruction execution. At that time, if an interrupt request is acknowledged by the ICU, the MCU is forced to follow the interrupt microprogram sequence.

Figure 1 shows the block diagram of the ICU. Interrupt requests pass through the interrupt request latch and priority encoder to the magnitude comparator. The output of the priority encoder is the binary equivalent of the highest active priority request. At the comparator, this value is compared with the Current Status (currently active priority level) contained in the current status latch. A request, if acknowledged at interrupt strobe time, will cause the interrupt flip-flop to enter the "interrupt active" state for one microinstruction cycle. This action causes the interrupt acknowledge (IA) signal to go low and sets the interrupt disable flip-flop.

The IA signal constitutes the interrupt command to the processor. It can directly force entry into the interrupt service routine as demonstrated in the appendix. As part of this routine, the microprogram normally reads the requesting level via the request level output bus. This information which is saved in the request latch can be enabled onto one of the processor input data buses using the enable level read input. Once the interrupt handler has determined the requesting level, it normally writes this level back into the current status register of the ICU. This action resets the interrupt disable flip-flop and acts to block any further request at this level or lower levels.

Entry into a macro level interrupt service routine may be vectored using the request level information to generate a subroutine address which corresponds to the level. Exit from such a macroprogram should normally restore the prior status in the current status latch.

The Enable This Level Group (ETLG) input and the Enable Next Level Group (ENLG) output can be used in a daisy chain fashion, as each ICU is capable of inhibiting interrupts from all of the following ICUs in a multiple ICU configuration.

The interrupt acknowledge flip-flop is set to the active LOW state on the rising edge of the clock when the following conditions are met:

- An active request level (R_0–R_7) is greater than the current status B_0–B_2
- The interrupt mode (ISE) is active
- ETLG is enabled
- The interrupt disable flip-flop is reset

When active, the IA signal asynchronously sets the disable flip-flop and holds the requests in the request latch until new current status information (B_0–B_2, SGS) is enabled (ECS) into the current status latch. The disable flip-flop is reset at the completion of this load operation.

During this process, ENLG will be enabled only if the following conditions are met:

- ETLG is enabled
- The current status (SGS) does not belong to this level group
- There is no active request at this level

The request level outputs A_0–A_2 and the IA output are open-collector to permit bussing of these lines in multi-ICU configuration.

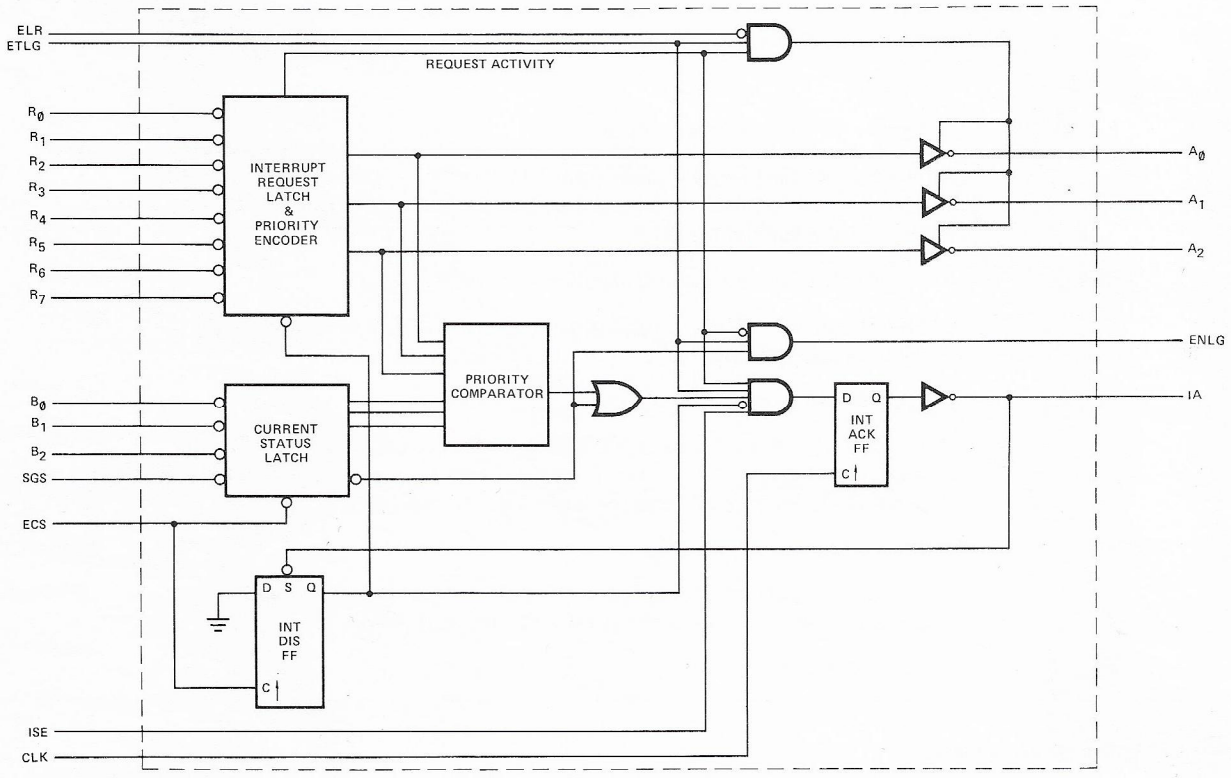


Figure 1. 3214 Block Diagram.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
- Ceramic . . . . . −65°C to +75°C
- Plastic . . . . . 0°C to +75°C

Storage Temperature . . . . . −65°C to +160°C

All Output and Supply Voltages . . . . . −0.5V to +7V

All Input Voltages . . . . . −1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +75°C

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP(1)	LIMITS MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (all inputs)				−1.0	V	I_C = −5 mA, V_{CC} = 4.75V
I_F	Input Forward Current:	ETLG input		−.15	−0.5	mA	V_F = 0.45V, V_{CC} = 5.25V
		all other inputs		−.08	−0.25	mA	
I_R	Input Reverse Current:	ETLG input			80	μA	V_R = 5.25V, V_{CC} = 5.25V
		all other inputs			40	μA	
V_{IL}	Input LOW Voltage:	all inputs			0.8	V	V_{CC} = 5.0V
V_{IH}	Input HIGH Voltage:	all inputs	2.0			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current			90	130	mA	V_{CC} = 5.25V(2)
V_{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I_{OL} = 15 mA, V_{CC} = 4.75V
V_{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I_{OH} = −1 mA, V_{CC} = 4.75V
I_{OS}	Short Circuit Output Current:	ENLG output	−20	−35	−55	mA	V_{OS} = 0V
I_{CEX}	Output Leakage Current:	IA and A_0–A_2 outputs			100	μA	V_{CEX} = 5.25V, V_{CC} = 5.25V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) B_0-B_2, SGS, CLK, R_0-R_4 grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS

T_A = 0°C to +75°C, V_{CC} = +5V ± 5%

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
t_{CY}	CLK Cycle Time	80			ns
t_{PW}	CLK, ECS, IA Pulse Width	25	15		ns
	Interrupt Flip-Flop Next State Determination:				
t_{ISS}	ISE Set-Up Time to CLK	16	12		ns
t_{ISH}	ISE Hold Time After CLK	20	10		ns
t_{ETCS}[2]	ETLG Set-Up Time to CLK	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After CLK	20	10		ns
t_{ECCS}[3]	ECS Set-Up Time to CLK (to clear interrupt inhibit prior to CLK)	35	25		ns
t_{ECCH}[3]	ECS Hold Time After CLK (to hold interrupt inhibit)	0			ns
t_{ECRS}[3]	ECS Set-Up Time to CLK (to enable new requests through the request latch)	110	70		ns
t_{ECRH}[3]	ECS Hold Time After CLK (to hold requests in request latch)	0			
t_{ECSS}[2]	ECS Set-Up Time to CLK (to enable new status through the status latch)	75	70		ns
t_{ECSH}[2]	ECS Hold Time After CLK (to hold status in status latch)	0			ns
t_{DCS}[2]	SGS and $B_Ø$-B_2 Set-Up Time to CLK (current status latch enabled)	70	50		ns
t_{DCH}[2]	SGS and $B_Ø$-B_2 Hold Time After CLK (current status latch enabled)	0			ns
t_{RCS}[3]	$R_Ø$-R_7 Set-Up Time to CLK (request latch enabled)	90	55		ns
t_{RCH}[3]	$R_Ø$-R_7 Hold Time After CLK (request latch enabled)	0			ns
t_{ICS}	IA Set-Up Time to CLK (to set interrupt inhibit F.F. before CLK)	55	35		ns
t_{CI}	CLK to IA Propagation Delay		15	25	ns
	Contents of Request Latch and Request Level Output Status Determination:				
t_{RIS}[4]	$R_Ø$-R_7 Set-Up Time to IA	10	0		ns
t_{RIH}[4]	$R_Ø$-R_7 Hold Time After IA	35	20		ns
t_{RA}	$R_Ø$-R_7 to $A_Ø$-A_2 Propagation Delay (request latch enabled)		80	100	ns
t_{ELA}	ELR to $A_Ø$-A_2 Propagation Delay		40	55	ns
t_{ECA}	ECS to $A_Ø$-A_2 Propagation Delay (to enable new requests through request latch)		100	120	ns
t_{ETA}	ETLG to $A_Ø$-A_2 Propagation Delay		35	70	ns
t_{IA}	$A_Ø$-A_2 Settling Time After IA		120	145	ns

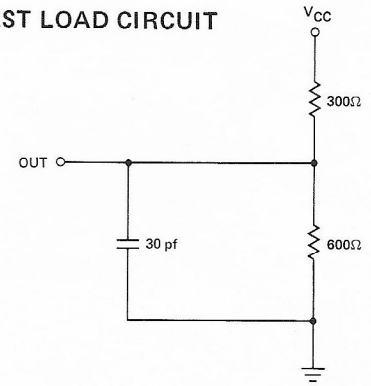
A.C. CHARACTERISTICS AND WAVEFORMS (cont.)

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
	Contents of Current Priority Status Latch Determination:				
t_{DECS}[4]	SGS and $B_\emptyset$-B_2 Set-Up Time to ECS	15	10		ns
t_{DECH}[4]	SGS and $B_\emptyset$-B_2 Hold Time After ECS	15	10		ns
	Enable Next Level Group Determination:				
t_{REN}	$R_\emptyset$-R_7 to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	ECS to ENLG Propagation Delay (enabling new request through the request latch)		85	90	ns
t_{ECSN}	ECS to ENLG Propagation Delay (enabling new SGS through status latch)		35	55	ns
t_{IEN}	ENLG Settling Time After IA		100	120	ns

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) Required for proper operation if ISE is enabled during next clock pulse.
(3) These times are not required for proper operation but for desired change in interrupt flip-flop.
(4) Required for new request or status to be properly loaded.

TEST CONDITIONS:
Input pulse amplitude: 2.5 volts.
Input rise and fall times: 5 ns between 1 and 2 volts.
Output loading of 15 mA and 30 pf.
Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT



CAPACITANCE(5)

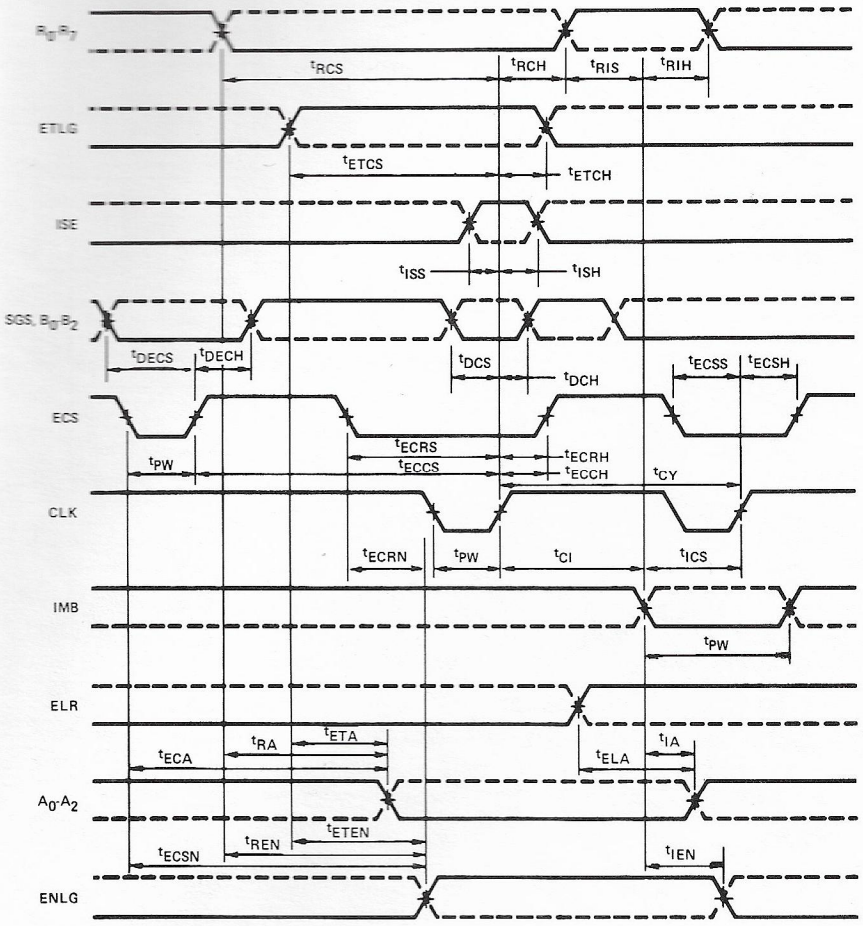
T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pf
C_{OUT}	Output Capacitance		7	12	pf

TEST CONDITIONS:
V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

NOTE:
(5) This parameter is periodically sampled and not 100% tested.

3214 WAVEFORMS



TYPICAL CONFIGURATIONS

The ICU has been designed for use with the INTEL Series 3000 Bipolar Microcomputer Set. It operates from the single common system clock and can accept an interrupt strobe (ISE) generated by the 3001 Micropgoram Control Unit or by a bit in microprogram memory as shown in Figures 2 and 3.

The ICU responds to interrupt requests of sufficient priority by entering the interrupt active mode. Its output (IA) can be tied to the row enable input (ERA) of the 3001 MCU. This gates an alternate row address onto the microprogram memory address bus which forces the system to execute an interrupt handling routine. Alternatively, the ICU output can be used to directly modify the MCU jump instruction (AC inputs) so that the next microprogram address corresponds to the start of the interrupt routine rather than the start of the macroinstruction fetch sequence. Of course, in the case of this particular implementation, the interrupt strobe must be generated one clock period earlier and the ISE output of the MCU should not be used.

As shown in Figure 4, when several ICUs are used together to provide a multiple of 8 priority levels, most control lines will be bussed. The Intel 3205 Decoder may be used to decode the high order bits of the request level, the information being derived from the daisy-chain group level signals.

As mentioned in the functional description, the request level information (A_0–A_2) may be sent to the 3001 MCU or the 3002 CP array as a constant through the Mask (K) bus or as data through the memory (M) or data (I) busses. Similarly, the status information can be generated by the CP array and carried to the ICU by the data (D) output bus of the CP array.

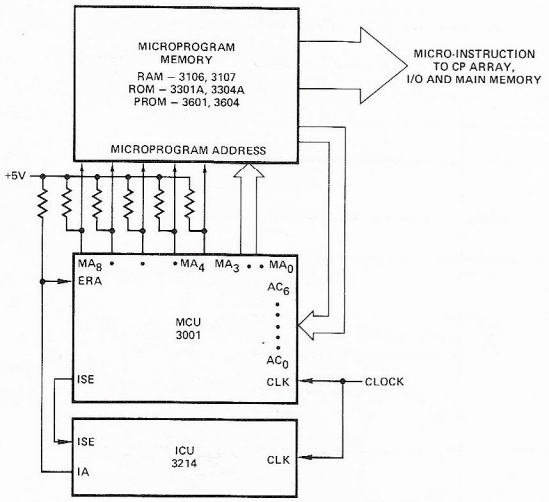


Figure 2. Interfacing 3214 with 3001.

Interrupt strobe generated by MCU.
Interrupt routine start address at column 15 row 31.
Macro-instruction fetch start address at column 15 row Ø.

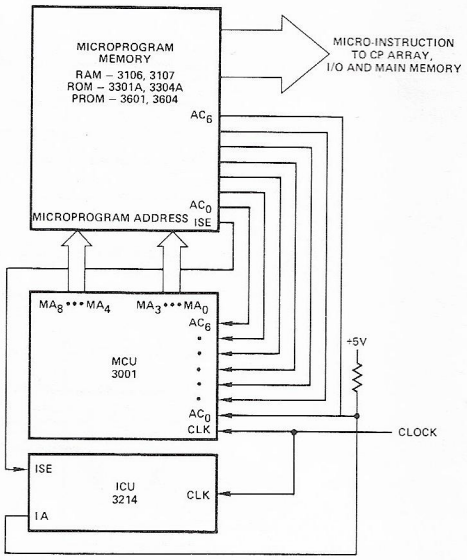


Figure 3. Interfacing 3214 with 3001.

Interrupt strobe generated by the microprogram memory.
Interrupt routine start address at column 14 row Ø.
Macro-instruction fetch start address at column 15 row Ø.

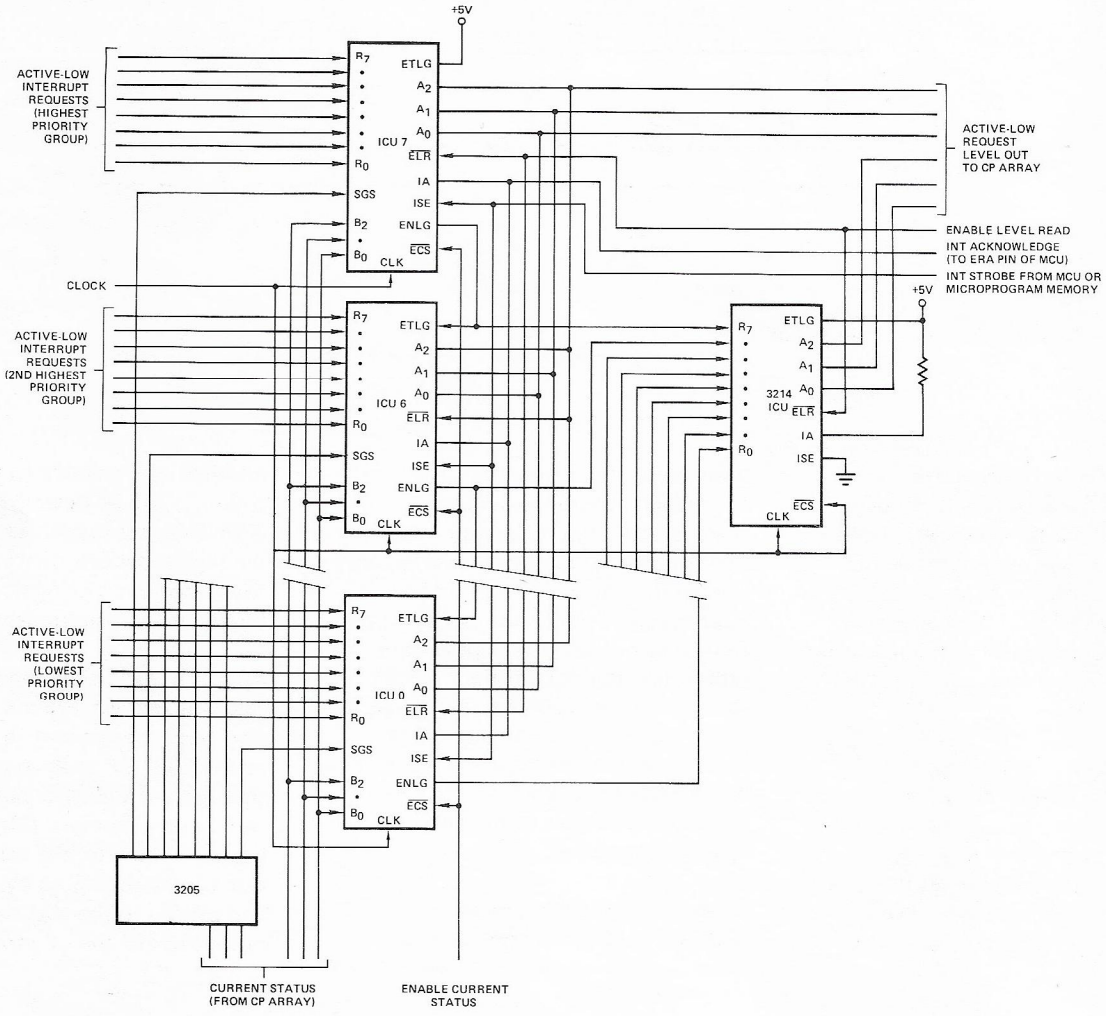


Figure 4. Using Several 3214 Interrupt Chips to Provide more than Eight Priority Levels. (The 3214 at the upper right is used to encode the high order bits of the requesting level)

ORDERING INFORMATION

Part Number	Description
P3214	Interrupt Control Unit

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